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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,485	11/05/2003	Le Trong Nguyen	SP015.C17	7752

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STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,485	NGUYEN ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-12,14-18 and 20-42* is/are pending in the application.

4a) Of the above claim(s) *1-7,13 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-12,14-18 and 20-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

01/07/04 02/17/04 08/30/04 07/11/05
01/23/04 03/24/04 10/20/04

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04/05/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 8-12,14-18, 20-42 are presented for examination. Claim 1-7,13,19 have been canceled. The copies of T.D. filed on 01/05/05 in regard to the copending cases and patents to avoid the double patenting rejections have been approved and received. However, new submissions of the T.D. are required in the continuation case.

2. The second IDS on 03/24/04 , which has the cited art of Walls, 4,879,787, with a different Serial Number, on the EDAN appears to be from a wrong case. Examiner has requested the docket area to verify the IDS entry. The applicant is suggested to confirm the right IDS on the same day, 03/24/04.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 8-12,14-18,25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al. (5,488,729) in view Yoshida (5,481,734).

2. As to claims 8,9,14, 20, Vegesna disclosed a superscalar processing system including at least :

a)a fetch circuit [IFETCH] for retrieving a plurality of instructions (see fig.19 [IFETCH], col.22, lines 25-38, col.23, lines 45-50, col.29, lines 6-13, col.30, lines 26-32);

b)an instruction buffer that buffers the plurality of instructions from fetch circuit(see fig.19 [DBUF], col.22, lines 25-38, col.23, lines 45-50, col.29, lines 6-13, col.30, lines 26-32);

c)plurality of functional units (see fig.18 [ALU][FAU][FMU]);

d)register file comprising at least temporary registers for storing execution results (see fig.18, [16][26], col.20, lines 34-67, col.21, lines 1-10, col.24, lines 10-20);

e) resource identifying circuit for identifying execution resources for a plurality of buffered instructions, and available for issue/fetch (see the instruction number at the fetch stage in fig.7);

f) issue control circuit for concurrent issuing more than one of the available instructions to the functional units (see the multiple instruction fetch at a given cycle 3 in fig.14(a));

g) a plurality of routing data paths coupled tote functional units and register file and configured to transfer result data from the function units to the register file (see feedback outputs 224 47 in fig.18);

h) bypass circuit configured to distribute data from the functional units tom other functional units via alternate path that bypasses the register file (see fig.6 for structure of bypass data bus, see the direct link of the output to the input port of functional units in fig.18);

i) renaming circuit configured to provide references to locations in the register file for logical register references included in the instruction (see the rename of the source and destination registers in col.13, lines 50-62);

j) branch prediction circuit (se col.11, lines 16-26).

3. Vegesna did not specifically show this routing data path transfer the result concurrently from more than one of the functional units to the register file as claimed. However, Yoshida taught a system including the transfer of result data simultaneously to a register file (col.2, lines 9-17, col.). It would have been obvious to one of ordinary skill in the art to use Yoshida in Vegesna for transferring the result data concurrently as claimed because the sue of Yoshida could provide Vegesna the ability to accept multiple data items at a single predefined style, thereby minimizing ht overall latency of the writeback cycle, and because Vegesna also taught concurrently identifying the execution resources for his plurality of buffered instructions (see the instruction number at the fetch stage in fig.7), which was a suggestion of the need for transferring the data results concurrently as clamed in order to adapt to the increased execution bandwidth of the plurality of buffered instructions , in doing so, provided a motivation.

4. As to clams 11,12, 17,18, see routing data paths in 224 47 in fig.18.

5. As to claims, 9,10, 15,16, see integer and floating pint functional units in fig.18.

6. As to clams 25-29, see the renaming and the source and destination registers in col.13, lines 50-62.

7. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al. (5,488,729) in view Yoshida (5,481,734) as applied to claims 8, 14 above, and further in view of Colwell et al. (5,446,912).

8. As to claims 20-24, neither Vegesna nor Yoshida disclose the retiring control logic as claimed., However, Colwell disclosed a system including retire control logic for storing result into temporary storage (see col.12, lines 60-68, col.13, lines 1-3). It would have been obvious to one of ordinary skill in the art to use Colwell in Vegesna for including retirement control as claimed because use of Colwell could provide Vegesna the capability to recover the data result after the completion of the retired instructions, and therefore, reducing the hardware overheads of the system, and because Vegesna did teach the division of the completion of his instruction execution in order to speed up the processing (see col.2, lines 1-19), which was an indication of the need for including the controlling processes of the termination of the instruction execution (e.g. retirement, or the like) for increasing the processing speed, for the above reason provided a motivation.

9. Claims 30-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani et al. (4,942,525) in view of Halo (4,594,655) .

10. As to claim 30,32-41, Shintani taught at least :

a) pre-fetching an instruction group including a plurality of instructions from a memory in a first processor cycle and holding the instruction group in a pre-fetch buffer (see col.7, lines 43-66), the pre-fetching accomplished so that instruction groups can be

retuned out of program order and subsequently reordered (see the rearrangement of instructions in col.7, lines 32-42 for the reorder);

b) transferring the instruction group held in the pre-fetch buffer to a multiple-stage buffer when there is a vacancy in the multiple-stage buffer with sufficient capacity to handle the instruction group as a unit (see the instruction buffer in col.7, lines 43-66);

c) simultaneously decoding, in a processor cycle after the first processor cycle, a plurality of instructions that are included in the instruction group, the decoding performed with at least one instruction at a predetermined position in multiple-stage buffer (see col.3, lines 41-57).

11. Shintani did not specifically show the checking of the dependencies and allocation of the instruction (see also the allocation of claim 41) as claimed. However, Hao disclosed a system for determining the dependencies and for allocating the instructions due to the instructions (see col.8, lines 27-59). It would have been obvious to one of ordinary skill in the art to use Hao in Shintani for including the checking of the dependencies and allocation of the instructions as claimed because the use of Hao could provide Shintani the ability to control the instruction sequence in a predetermined set of parameters, such as the dependencies, and because Shintani also taught miswritten result of a prediction , and a recovery thereof was necessary (see col.1, lines 25-35), which was a suggestion of the desirability to include the dependency checking in order to prevent the miswritten result on prediction , for the above reasons, provided a motivation.

12. As to the removing of the instructions , see Shintani's extraction of instructions from the instruction buffer in col.7,lines 67-68,co.8, lines 1-4).

13. As to the simultaneous transfer of the instructions in claims 31, see Shintani's simultaneous transfer in col.3, lines 41-57.

14. As to the retirement of the instructions, see Shintani's completion of the execution cycle in col.5, lines 65-68, col.6, lines 1-7).

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Hasbrouck et al. (3,718,912) is cited for showing the teaching of selecting temporary registers by renaming the specified storage means and assigning them to specific instructions (See Col.2, lines 54-61).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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